Specification Amendments

Amend the title as follows:

FIELD PROGRAMMABLE GATE ARRAY HAVING ~~PARTITONABLE~~ EMBEDDED MEMORY WITH CONFIGURABLE DEPTH ~~VERSUS~~ AND WIDTH

Amend the paragraphs noted below as follows:

[0001] This application is a continuation-in-part (CIP) of U.S. Application No. ~~xx~~10/406,050 ~~[Attorney Docket No. LATC-01048us0]~~ filed April 2, 2003 by Om P. Agrawal et al. where the latter is a continuation-in-part (CIP) of U.S. Application No. 10/194,771 ~~[Attorney Docket No. LATC-01046us0]~~ filed July 12, 2002 by Om P. Agrawal et al. and this application incorporates by reference the disclosure of each of said parent applications.

[0002] The following copending U.S. patent applications are owned by the owner of the present application, and their disclosures are incorporated herein by reference:

[0003] (A) Ser. No. 10/406,050 ~~[Attorney Docket No. LATC-01048us0]~~ filed April 2, 2003 by Agrawal et al., and originally entitled, "Hierarchical General Interconnect Architecture for High Density FPGA'S", which application is also a CIP of below-cited U.S. application Ser. No. 10/194,771; and

[0004] (B) Ser. No. 10/194,771 ~~[Attorney Docket No. LATC-01046us0]~~ filed July 12, 2002 by Om P. Agrawal et al.

Delete the following paragraph that appears at the beginning of page 41 of the application:

~~[Note: Square bracketed and small-sized cross-referencing text is provided in the below application claims as an aid for readability and for finding corresponding (but not limiting) examples of support in the specification. The bracketed text (e.g., [100] is not intended to add any limitation whatsoever to the claims and should be deleted in all legal interpretations of the claims and should also be deleted from the final published version of the claims.]~~